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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,855	09/26/2000	John Michael Brown	20206-081 (TA-490)	6646

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Intellectual Property Administration
Legal Department, M/S 35
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	18

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/670,855	BROWN, JOHN MICHAEL	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amndt C filed on 1/23/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 25-27* is/are allowed.

6)☒ Claim(s) *10-12,15,17-24* is/are rejected.

7)☒ Claim(s) *13,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to the applicant's amendments

****** The examiner considers the preliminary amendment filled on 01/23/04.

******Claim 9, which was previously allowed in paper number 14, is allowed.

*******New added claims, 10-27 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims **17 and 24** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included and excluded by the claim language with the use of the phrase: "approximately the same time". This claim is an omnibus type claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **10-12, 15, 18-24** are rejected under 35 U.S.C. 102 (b) as being clearly anticipated by Ruparel (U.S. PN: 5,689,517).

As per claim **10,** Ruparel in figure (1b) teaches or discloses a circuit (see element 15) comprising a first clock domain (10a) comprising first edge triggered memory device (11a) for

receiving first data input signal (see SCAN-IN input and clock signal CLK A) to produce first output signal and coupled to a first latch (12a) for outputting first output signal; second clock domain (10b) comprising a second edge triggered memory device (11b) for receiving a second input data and to produce third output signal (see line between 11b and 12b) coupled to a second latch (12b) for outputting forth output signal (see the line L2).

As per claim **11,** Ruparel in figure (1b) teaches all the subject matter claimed in claim 1 including Ruparel teaches that the first and second edge triggered memory devices as flip-flops or latches (see figure 1b, elements 11a and 11b).

As per claim **12,** Ruparel in figure (1b) teaches all the subject matter claimed in claim 1 including Ruparel teaches that the first data input signal comprises a scan input data in (see fig. 1b, line SCAN-IN).

As per claims **15 and 17,** Ruparel in figure (1b) teaches all the subject matter claimed in claim 1 including Ruparel teaches a third clock domain for receiving a fourth output signal (see element 11c).

As per claim **18,** Ruparel in figure (1b) teaches or discloses plurality of clock domains (see 10a-10c) coupled to each other through a test path (see the connections between the clock domains (SCAN-IN to SCAN-OUT)) to receive a functional data and a clock signal (see SCAN-IN and CLK A and CLK B) wherein each of the clock domain comprises a test clock and a test data (see SCAN-IN and CLK A and CLK B) for producing an output data (SCAN-OUT). Although, Ruparel does not explicitly teach test selection input (multiplexer) for enabling test mode, this feature is deemed to be inherent to the system of Ruparel since Ruparel in column 2 lines 47-65 teach that most widely adopted scan technique is the mux-type-scan-D-flip-flop

shown in figure 2a in which multiplexer (21) is used with D-flip-flop (22) and D-flip-flop (22) is typically a conventional D-flip-flop consisting of a master latch and a slave latch that operate together in response to a system clock and further the multiplexer (21) is connected to the input of D-flip-flop (22) to enable the mux-type-scannable-D-flip-flop (20) to select either Data-In input or Scan-In input by using a scan enable control signal (SE) (see col. 2, lines 47-65).

As per claims **19-23,** Ruparel in figure (1b) teaches all the subject matter claimed in claim 18 including Ruparel teaches the scannable-D-flip-flop is comprised of two master latches and one slave latch such that the scannable-D-flip-flops may operate in a normal mode of operation or a scan/test mode of operation. During normal mode of operation, the first master latch operates together with the slave latch in response to the system clock and during the scan/test mode of operation; the second master latch operates together with the slave latch in response to a scan clock (see abstract).

As per claims **24,** Ruparel in figure (1b) teaches all the subject matter claimed in claim 1 including Ruparel teaches a third clock domain for receiving a fourth output signal (see element 11c).

Allowable subject matter

3. Claims **13, 14 and 16,** are objected to as being dependent upon a rejected base claim but would be allowable if rewritten independent from including all of the limitation of the base claim and any intervening claims. The claimed invention comprises a combinatorial logic configured to receive each of a functional data signal and the second output signal from the first latch and configured to produce a combinatorial logic output signal and a multiplexer configured to

receive each of the combinatorial output signal and a scan data input signal **(as in claim 13)** which the prior art do not teach or render obvious.

The circuit wherein the second clock domain is configured to receive the second output signal from the first latch at a multiplexer **(as in claim 14)** which the prior art do not teach or render obvious.

The circuit wherein the third clock domain comprises a multiplexer configured to receive the fourth output signal from the second latch, a third edge triggered memory device configured to receive a third data input signal from the multiplexer, and configured to produce a fifth output signal in response to a third clock signal and combinatorial logic configured to receive each of a functional data signal and the fifth output signal from the third edge triggered device and configured to produce a combinatorial logic output signal, wherein the combinatorial output signal is delivered to the multiplexer **(as in claim 16)** which the prior art do not teach or render obvious.

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

4. Claims **25 to 27** have been allowed.

As per claim **25,** the prior arts (U.S. PN: 5,689,517, 6,131,173 and 6,418,545) of record teach a method of testing circuit comprising a plurality of clock domains each domains receive a clock signal, operate a test mode when a test mode is asserted (to cause a signal line to make a transition from false state to true state) or de-asserted. However, the prior arts taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method of executing the first

shift cycle in the circuit, wherein executing the shift cycle comprises asserting a test mode signal wherein assertion of the test mode signal configures a first edge triggered device to receive test data from a test data input and configures each of a plurality of second edge triggered devices in the system to receive data serially from a respective one of the first and the plurality of second edge triggered devices: de-asserting the clock signals to each of the clock domains; simultaneously asserting each of the clock signals to shift the test data into the first edge triggered device and de-asserting the test mode signal, such that the circuit operates in the functional mode and executing a sample cycle in the circuit, wherein executing the sample cycle comprises: de-asserting each of the clock signals; delivering test data to the first edge triggered device; de-asserting the test mode signal, thereby placing the circuit in the functional mode; delivering test data to the first edge triggered device and each of the plurality of second edge triggered devices; asserting the test clock to hold data on an output of each of the plurality of latches and at an input of each of the plurality of second edge triggered devices and simultaneously asserting each of the clock signals. Consequently, claim 25 is allowed over the prior art.

Claims **26 and 27,** which are directly or indirectly dependents of claim 25 are also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,131,173 Meirlevede et al.

US PN: 6,418,545 Adusumilli

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
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